REMARKS

By this Amendment, claims 1-8 are amended, and claims 9-10 are added. Thus, claims 1-10 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

The specification and abstract have been carefully reviewed and revised in order to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification and abstract.

In item 2 on page 2 of the Office Action, claims 1-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong et al. (U.S. 5,696,953) in view of Conary et al. (U.S. 5,842,029). This rejection is respectfully traversed for the following reasons.

The present invention, as recited in claim 1, provides a multiple power source semiconductor integrated circuit which includes a plurality of function blocks that are supplied with power from a different one of a plurality of power supply circuits, respectively, and a microcomputer for controlling the supply of power to the plurality of function blocks, where the microcomputer is one of the plurality of function blocks. In addition, the multiple power source semiconductor integrated circuit of the present invention includes a power supply control circuit for controlling the supply of power by the plurality of power supply circuits under the control of the microcomputer.

According to this construction, the present invention produces novel and advantageous effects in that it becomes possible to reduce unnecessary power consumption that is generated by a static power supply current (leak current) which flows statistically even when clocks are halted by halting the supply of power to the function blocks which are not being used according to a control signal from a microcomputer, which is one of the plurality of function blocks that are integrated on a multi-power supply semiconductor integrated circuit.

Furthermore, the present invention produces other novel and advantageous effects in that it becomes possible to reduce unnecessary power consumption that is generated due to a static power supply circuit which flows statistically in the microcomputer by halting the supply of power to the microcomputer itself according to a control signal from the microcomputer when the microcomputer is in a standby state.

Accordingly, unlike conventional systems such as Wong et al. and Conary et al. which aim to reduce unnecessary power consumption merely by controlling the supply of clocks to reduce operation power supply current, the multiple power source semiconductor integrated circuit recited in claim 1 controls the supply of power from a plurality of power supply circuits to a plurality of function blocks to reduce a static power supply current.

Wong et al. discloses an apparatus and method for managing power consumption of an integrated circuit which includes a microprocessor, a plurality of function blocks and a clock generator circuit. The clock generator circuit supplied clocks to the respective function blocks according to a control signal from the microprocessor. Accordingly, Wong et al. reduces operation power supply current and unnecessary power consumption merely by halting the supply of clocks to the function blocks which are not in use, according to the control signal from the microprocessor.

Therefore, the only similarity between Wong et al. and the multiple power source semiconductor integrated circuit of claim 1 is that power consumption is suppressed under the control of a microprocessor (microcomputer). Accordingly, while Wong et al. controls the supply of clocks to the respective function blocks, the multiple power source semiconductor integrated circuit of claim 1 is recited as controlling supply of power to the plurality of function blocks, which is markedly different from controlling the supply of clocks to the respective function blocks.

Consequently, even if Wong et al. can halt the supply of clocks to the respective function blocks to suppress power consumption, Wong et al. cannot achieve the effects of the multiple power source semiconductor integrated circuit of claim 1 of controlling the supply of power to the function blocks to reduce power consumption due to a static power supply current which flows statistically.

Conary et al. discloses an apparatus and method for powering down an integrated circuit which includes a microprocessor and a clock generator circuit that supplies clocks to the microprocessor according to a control signal from the microprocessor. Accordingly, similar to Wong et al., Conary et al. reduces operation power supply current and unnecessary power consumption merely by halting the supply of clocks to the microprocessor according to a program when the microcomputer is not in use and is in a standby state.

Therefore, the only similarity between Conary et al. and the multiple power source semiconductor integrated circuit of claim 1 is that power consumption is suppressed under the control of a microprocessor. However, while Conary et al. controls the supply of clocks to the microprocessor based on a control signal from the microprocessor, the multiple power source semiconductor integrated circuit of claim 1 defines that the microprocessor is one of the plurality of function blocks and that the supply of power to the plurality of function blocks is controlled. Therefore, the multiple power source semiconductor integrated circuit of claim 1 controls the supply of power to the microprocessor itself, which is markedly different from controlling the supply of clocks to the microprocessor.

Accordingly, the combination of Wong et al. and Conary et al. merely result in an apparatus that controls the supply of clocks to a plurality of function blocks including a microprocessor. On the other hand, the multiple power source semiconductor integrated circuit of claim 1 is recited as controlling the supply of power to the plurality of function blocks including the microprocessor in order to reduce power consumption due to a static power supply current which flows statistically.

Therefore, no obvious combination of Wong et al. and Conary et al. would result in the invention of claim 1 since Wong et al. and Conary et al., either individually or in combination, do not disclose or suggest that the supply of power to the plurality of function blocks including the microprocessor is controlled, as recited in claim 1.

Because of the clear distinctions discussed above, it is submitted that the teachings of Wong et al. and Conary et al. clearly do not meet each and every limitation of claim 1.

Furthermore, it is submitted that the clear distinctions discussed above are such that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify Wong et al. and Conary et al. in such as manner as to result in, or otherwise render obvious, the present invention as recited in claim 1.

Therefore, it is submitted that the claim 1, as well as claims 2-10 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

Kazuya TANIGUCHI et al.

By: _____
Jonathan R. Bowser
Registration No. 54,574
Attorney for Applicants

JRB/nrj
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
March 28, 2006